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REMARKS

Claims 2 – 9, 11 – 18 and 23 – 24 and 26 - 35 are pending. Claims 2, 6, 15, 17, 23 – 24, 26, and 28 – 29 and 31 – 32 are currently amended. Claims 22 and 25 are currently cancelled and claims 1, 10, 19 – 21 were previously cancelled. No new matter has been added. Reconsideration is requested.

CLAIM OBJECTIONS

Claims 22 – 28 were objected to for being of improper dependent form. Applicants have amended claims 23 – 24 and 26 – 28 accordingly. Claims 22 and 25 have been cancelled.

Claim 31 was objected to and has been amended accordingly.

Claim 32 was objected to for an unclear recitation of "critical interconnect lines" and "transmission line topologies". Claim 32 has been amended to clarify the relationship of the critical interconnect lines and the transmission line topologies.

Chao et al

Claims 2 – 7 and 15 – 18 were rejected under 35 U.S.C. 102(b) as being anticipated by Chao et al. (US patent 5,031,111). Applicants respectfully traverse the Examiner's rejection.

Chao discloses microwave and millimeter ware and the like, and does not disclose AMS, as is recited in amended claims 2, 6, 15 and 17.

Microwave and AMS are different technologies, and, as such, microwave design techniques cannot be transferred to AMS design techniques. Microwave and AMS transmission line topologies are also different topologies and are not transferable.

Microwave transmission line wires and shielding are very, very thin and semi-infinitely wide. In models of microwave transmission line topology, the wires and shielding are calculated with a thickness of zero. Since the thickness is estimated at zero, calculations of microwave transmission line topologies do not include factors of resistance, except in instances of calculations of energy loss. Additionally, since the width of the wires and shielding is semi-infinitely wide, their shape is calculate as a plane.

In contrast, as illustrated in Figs. 3 and pages 13 – 20 of the present application, design of the AMS transmission line topologies is a complex, difficult

calculation. The thickness and width of the wires and shielding vary and cannot be assumed to be either zero or semi-infinite.

Thus, Chao et al. does not teach "designing one or more transmission lines for analog and mixed signal (AMS) circuit design", as recited in currently amended claim 2, or "AMS transmission lines" as recited in currently amended claim 6. Applicants respectfully submit that currently amended claims 2, 6, 15 and 17 are allowable over Chao et al. and claims 3 – 5, 7, 9, 16, and 18, dependent therefrom, are allowable over Chao et al.

Chang et al

Claims 2 – 9, and 11 – 18 were rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (Publication No: US 2002/0104063). Applicants respectfully traverse the Examiner's rejection. Chang does not design transmission lines; Chang extracts and analyzes the already existing transmission lines. Chang does not have a design tool; Chang has an extraction and analysis tool.

Chang describes in Fig. 1 the design methodology, step 101, "specify the functional and logic designs", step 102, "synthesize" and step 103, "timing analysis" are following by step 104, "physical design" (paragraph 0005). Chang states that step 104 includes placing and routing (step 201), and then, extraction of parasitic impedance (step 202) (paragraph 0006).

In the Summary, Chang states, "A need has arisen for a method and system for extracting parasitic interconnect impedances, including inductance. Accordingly a novel parasitic extraction system is disclosed." (paragraphs 0010- 0011). As Chang describes, the parasitic extraction system is part of step 202, which comes after steps 101 – 103 (Fig. 1). Chang's invention is only operative once the design is already completed. In paragraph 0006, Chang states, "At step 202, estimate of the parasitic impedances of lines in the physical implementation are made ("extracted") to form an interconnect delay model". Chang is thus extracting and analyzing the physical implementation of an already designed and already existing circuit.

Thus, Chang does not teach "means for designing one or more transmission line topologies" (currently amended claims 2), or "A design topology" (currently amended claims 6 and 15), or "designing topology of transmission lines" (currently amended claim 17).

Applicants respectfully submit that currently amended claims 2, 6, 15 and 17 are allowable over Chang et al. In view of the allowability of claims 2, 6, 15 and 17,

claims 3 – 5, 8 – 9, 11 – 14, 16, and 18 dependent therefrom are also believed to be allowable.

Dangelo et al.

Claim 30 has been rejected under 35 U.S.C. 103(b) as being anticipated by Dangelo et al. (US patent 5,555,201). Applicants respectfully traverse the Examiner's rejection. Dangelo does not differentiate between critical and non-critical interconnect lines.

Dangelo teaches digital technology, (column 1, line 42) which is interested in time delay, but not in signal quality. As the Examiner very correctly pointed out, Dangelo in column 20, lines 10 – 13 finds it "necessary to use a floor planner or placement and routing programs to estimate wire delays". Dangelo's floor planner 710 (column 22, lines 38 – 48) is used "to re-estimate the internal wire delays ..." .

However, at no point does Dangelo discuss that "some interconnect lines are critical, namely their non-ideal behavior has a large effect on performance, and other may not be" (page 9 to present application). Digital technology is not concerned with non-ideal behavior, and thus Dangelo does not have any incentive to find the critical wires. Dangelo treats all the wires the same.

Thus, Applicants respectfully submit that Dangelo does not "define one or more critical interconnect lines" and that claim 30 is allowable over Dangelo et al

Pileggi et al.

Claim 30 has been rejected under 35 U.S.C. 102(e) as being anticipated by Pileggi et al. (US patent 6,367,051). Applicants respectfully traverse the Examiner's rejection. Pileggi does not differentiate between critical and non-critical interconnect lines.

Similar to Dangelo, Pileggi is also interested in time delay and not in signal quality. Pileggi states in column 2, lines 51 – 55, "The present invention provides a method that inserts buffers concurrently with placement optimization. The buffers are inserted to avoid excessive signal attenuation and to reduce delay...".

At no point does Pileggi discuss the issue of critical vs non-critical lines; he has no incentive to do so. Rather, Pileggi treats all the wires the same, "Having mapped all circuit elements into bins, delays for each bin is calculated." (step 4, column 3, lines 62 – 63).

Thus, Applicants respectfully submit that Pileggi et al. does not "define one or more critical interconnect lines" and that claim 30 is allowable over Pileggi et al.

Chang et al. over Pileggi et al

Claims 22 - 32 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (Publication No: US 2002/0104063) in view of Pileggi et al. (US patent 6,367,051).

Applicants respectfully traverse the Examiner's rejection of claim 31. As argued above, Chang does not design transmission line topologies; rather Chang extracts and analyzes an already existing physical layout.

Thus, as argued above, Chang does not teach "means for designing a high level circuit design... and further including one or more transmission line topologies".

Pileggi does not provide "means for designing a high level circuit design... and further including one or more transmission line topologies". Rather, as the Examiner very correctly noted, Pileggi states, "The present invention provides a method for mapping circuit of elements of a net list onto a physical design" (column 1, lines 45 – 67)

The Examiner also helpfully pointed out column 3, lines 30 – 60 "The circuit elements of the net list are then clustered or grouped according to a floor plan". Pileggi does not create the floor plan including the transmission line topologies; he generates the physical layout as described in the previously designed floor plan.

Therefore, neither Chang et al., nor Pileggi et al., nor the combination of the two teach "means for designing a high level circuit design... and further including one or more transmission line topologies", and as such claim 31 is allowable over the combination of Chang et al. and Pileggi et al.

As to claim 32, the Applicants respectfully traverse the Examiner's rejection. As argued above, Chang treats all of the interconnects to the same extraction and analysis without regard to those that may be more critical than others.

Furthermore, as argued above, Pileggi does not define one or more critical interconnect lines.

Therefore, neither Chang et al., nor Pileggi et al., nor the combination of the two perform the step of "identifying one or more critical interconnect lines". As such claim 32 is allowable over the combination of Chang et al. and Pileggi et al. Arugments for claim 30 are given above. In view of the allowability of claim 30 – 32, claims 22 – 29 dependent therefrom are also believed to be allowable.

Chang et al

Claims 34 and 35 have been rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (Publication No: US 2002/0104063). Applicants respectfully traverse the Examiner's rejection. Chang does not design; Chang extracts and analyzes. Chang does not have a design tool; Chang has an extraction and analysis tool.

Applicants have argued above, and will not repeat herein the entire argument that Chang does not teach " designing a schematic design... including one or more transmission wire models", nor does he teach "designing a physical layout including ...one or more transmission line topologies". Thus, Applicants respectfully submit that claims 34 and 35 are allowable over Chang et al.

Applicants believe that the above amendments and remarks are fully responsive to all the objections and grounds of rejections by the Examiner. In view of the foregoing amendments and remarks, the Applicants respectfully submit that all the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fee associated with this paper to Deposit Account No. 09-0468.

Respectfully submitted,

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